



UNITED STATES PATENT AND TRADEMARK OFFICE

55
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,616	10/14/2003	Erwin B. Cohen	BUR920020099US1	2615
23389	7590	12/29/2005		EXAMINER
SCULLY SCOTT MURPHY & PRESSER, PC				FARROKH, HASHEM
400 GARDEN CITY PLAZA				
SUITE 300			ART UNIT	PAPER NUMBER
GARDEN CITY, NY 11530				2187

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/605,616	COHEN ET AL.
	Examiner	Art Unit
	Hashem Farrokh	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 27 October 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 2-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 2-19 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 14 October 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

This Office Action is in response to the Applicants' Remarks dated 10/27/05. The instant application having application No. 10/605,616 has a total of 18 claims pending in the application; claims 2, 5, 7-10, 16, and 19 have been amended; claim 1 has been canceled; no new claims have been added.

INFORMATION CONCERNING CLAIMS:

The indicated allowability of some of the claims is withdrawn in view of the newly discovered reference(s). The Examiner apologizes if this will cause any inconvenience.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,845,432 B2 to Maiyuran et al. (hereinafter Maiyuran).

1. *In regard to claim 19, Maiyuran teaches:*

"A method of operating a power saving cache" (e.g., see abstract; column 1, line 67; column 2, lines 1-5).

"comprising:"

"using circuitry to dynamically reduce the logical size of the cache in order to save power;" (e.g., see abstract; column 1, lines 65-67; column 2, lines 1-5; elements 140 and 180 in Fig. 1).

"wherein the using step includes the step of partitioning the cache in one of given number of ways to provide a desired configuration and granularity," (e.g., see column 2, lines 9-10; Figs. 1 and 5).

"said given number of ways comprising (i) equal sized partition," (e.g., see column 9, lines 34-38; Fig. 5). For example Maiyuran teaches that partition may be in equal or different sizes.

"and binary weighted with or without a constantly powered way." (e.g., see column 1, line 67 and column 2, lines 1-5). Maiyuran teaches each module or partition may be powered down independently. The ability to power off/on cache partitions represents the binary-weighted powered way (e.g., see Fig. 7 of Applicants' specification).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maiyuran in view of U.S. Patent No. 6,421,809 B1 to Wuytack et al. (hereinafter Wuytack).

2. *In regard to claims 2, Maiyuran teaches:*

"A power saving cache" (e.g., see abstract; column 1, line 67; column 2, lines 1-5).

"comprising."

"circuitry (e.g., see elements 140 and 180 in Fig. 1) to dynamically reduce the logical size of the cache in order to save power;" (E.g., see abstract; column 1, lines 65-67; column 2, lines 1-5). Maiyuran teaches that by powering down cache modules and/or enabling cache modules based on microinstruction-by-microinstruction (UOP-by-UOP) bases, the cache power consumption can be reduced. Powering down and/or disabling parts of cache circuits that are not participating in cache operations represent dynamically reducing the cache logical size as recited in the claim. However, Maiyuran does not expressly teach: "means for determining an optimal cache size for balancing power and performance."

Wuytack teaches: "means for determining an optimal memory size for balancing power and performance." (e.g., see column 6, lines 43-47) for determining an optimized memory organization (how many memories, which size for each memory, interconnection patterns of said memories), such that the digital device can run with optimal performance (for instance with minimal power consumption).

Disclosures by Maiyuran and Wuytack are analogous because both references teach methods of dynamically reducing memory size to save power in memory devices.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the low power cache architecture taught by Maiyuran to include optimization method for optimizing performance (including saving power) disclosed by Wuytack.

The motivation for using optimization method as taught by column 6, lines is to enable a digital device run with optimum performance.

Therefore, it would have been obvious to combine disclosures by Wuytack and Maiyuran to obtain the invention as specified in the claim.

3. *In regard to claim 3, Wuytack further teaches:*

"wherein the means for determining an optimal cache size includes hardware means." (e.g., see column 30, lines 51-53). For example Wuytack discloses that to perform the optimization technique, in addition to a suitable computer, a second computing device for selecting an optimized memory organization (e.g., hardware mean) is used.

4. *In regard to claim 4, Wuytack further teaches:*

"wherein the means for determining an optimal cache size includes software means." (e.g., see column 30, lines 45-47). For example the use and execution of computer instructions to determine optimized scheduling is the software means.

5. *In regard to claim 5, Maiyuran teaches:*

"further comprising means for maintaining coherency of data in the cache as the size of the cache is altered." (e.g., see column 2, lines 16-17).

6. *In regard to claim 6, Maiyuran teaches:*

"wherein some of the data in the cache is modified data (e.g., see column 4, lines 16-17), and the means for maintaining coherency includes means for handling said modified data." (e.g., see column 2, lines 16-17; column 5, lines 12-26). For example cache coherency handled by using the cache state information.

7. *In regard to claim 7, Maiyuran teaches:*

"wherein the circuitry includes means for partitioning the cache in one of several ways to provide a desired configuration and granularity." (e.g., see column 2, lines 9-10; Figs. 1 and 5). For example the cache organized (e.g., partitioned) in set of ways.

8. *In regard to claim 8, Maiyuran teaches:*

"wherein the circuitry includes means to power off sections of the cache." (E.g., see column 1, lines 67; column 2, line 1).

9. *In regard to claim 9, Maiyuran teaches:*

"wherein the cache is a set associative cache with N-ways, and the circuitry includes means to partition the cache along said ways." (E.g., see column 2, lines 9-10; Figs. 1 and 5-6).

10. *In regard to claim 10, Maiyuran teaches:*

"A method of operating a power saving cache comprising:" (e.g., see abstract; column 1, line 67; column 2, lines 1-5).

"using circuitry (e.g., see elements 140 and 180 in Fig. 1) to dynamically reduce the logical size of the cache in order to save power." (e.g., see abstract; column 1, lines 65-67; column 2, lines 1-5). Maiyuran teaches that by powering down cache modules and/or enabling cache modules based on microinstruction-by-microinstruction (UOP-by-UOP) bases, the cache power consumption can be reduced. Powering down and/or disabling parts of cache circuits that are not participating in cache operations represent dynamically reducing the cache logical size as recited in the claim. However, Maiyuran does not expressly teach: "determining an optimum size for the cache for balancing power and performance given a set of power and performance criteria."

Wuytack teaches: "determining an optimum size for the memory for balancing power and performance given a set of power and performance criteria." (e.g., see column 6, lines 43-47) for determining an optimized memory organization (how many memories, which size for each memory, interconnection patterns of said memories), such that the digital device can run with optimal performance (for instance with minimal power consumption). Wuytack teaches the power (e.g., power cost) is an input (e.g., a criterion for determining the optimized memory performance using a control flow graph model. The motivation for combining the two references is based on the same rational given in rejection of claim 1.

11. In regard to claim 11, Maiyuran teaches:

"wherein the cache is a set associative cache including N-ways, and the step of using circuitry to dynamically reduce the logical size of the cache includes the step of using the circuitry to partition the cache along the ways." (**E.g., see column 2, lines 6-50; Figs.1).**

12. *In regard to claim 12, Maiyuran teaches:*

"wherein each of said N ways is individually powered." (**E.g., see abstract; column 1, line 67; column 2, line 1).**

13. *In regard to claim 13, Maiyuran teaches:*

"wherein the cache includes data, and the method comprises the further step of maintaining integrity of the data as the size of the cache is altered." (**E.g., see column 4, lines 14-26).** *Maiyuran teaches that dirty data (e.g., modified data) is protected when some ways are being disabled to save power. The data integrity is maintained by using state information.*

14. *In regard to claim 14, Maiyuran teaches:*

"step of powering off sections of the cache." (**E.g., see column 4, lines 21-24).** *Maiyuran teaches that victim way (e.g., way containing dirty or modified) data may be enabled. All other ways may be powered down.*

15. *In regard to claim 15, Maiyuran teaches:*

"wherein some of the data in the cache is modified data, and the step of maintaining integrity of the data includes the step of, before powering off one of the sections of the cache, saving any modified data in said one section of the cache." (e.g., see column 4, lines 18-24). *The way that contains the modified or dirty data is enabled (e.g., not powered down). All other ways are powered down.*

16. *In regard to claim 16, Maiyuran teaches:*

"A method of operating a power saving cache," (e.g., see abstract; column 1, line 67; column 2, lines 1-5).

"wherin the cache includes data and some of the data in the cache is modified data," (e.g., see column 4, lines 16-17).

"the method comprising:"

"using circuitry to dynamically reduce the logical size of the cache in order to save power;" (e.g., see abstract; column 1, lines 65-67; column 2, lines 1-5; elements 140 and 180 in Fig. 1).

"maintain integrity of the data as the size of cache is altered;" (e.g., see column 2, lines 16-17; column 5, lines 12-26). *For example maintaining cache coherency taught by Maiyuran is for maintaining the integrity of data as is recited in the claim.*

"powering off sections of the cache;" (e.g., see column 1, line 67 and column 2, lines 1-5).

"wherin the step of maintaining integrity of the data includes the step of before powering off one of the sections of the cache, saving any modified data in said section of cache;"

(e.g., see column 4, lines 18-24). *The way that contains the modified or dirty data is enabled (e.g., not powered down). Therefore, dirty or modified data is being saved.*

However, Maiyuran does not expressly teach: "further comprising the step of determining an optimum size for the cache given a set power and performance criteria, and wherein the step of using circuitry includes the step of using circuitry to reduce the size of the cache to said optimum size."

*Wuytack teaches: "further comprising the step of determining an optimum size for the memory given a set power and performance criteria, and wherein the step of using circuitry includes the step of using circuitry to reduce the size of the cache to said optimum size." **(e.g., see column 6, lines 43-47)** for determining an optimized memory organization (how many memories, which size for each memory, interconnection patterns of said memories), such that the digital device can run with optimal performance (for instance with minimal power consumption). The motivation for combining the two references is based on the same rational given in rejection of claim 1.*

17. *In regard to claim 17, Wuytack further teaches:*

*"wherein the step of determining an optimum size includes the step of using one of a predefined set of hardware techniques to determine said optimum size." **(e.g., see column 30, lines 51-53)**. For example Wuytack discloses that to perform the*

optimization technique, in addition to a suitable computer, a second computing device for selecting an optimized memory organization (e.g., a predefined set of hardware) is used.

18. *In regard to claim 18, Maiyuran further teaches:*

"wherein the cache is used in a processor," (e.g., see abstract).

"and the method includes the further steps of: running on the processor a cache size adjustment routine;" (e.g., see column 4, lines 45-63). For example Maiyuran teaches when a cache write instruction is a cache hit, the new data will be written to the tag field and data field of the cache entry that cause the hit. All other ways and victim allocation unit may be powered down (e.g., the cache logical size being adjusted). However, Maiyuran does not expressly teach: "and feeding information to said routine to determine the optimum size of the cache."

Wuytack teaches: "and feeding information to said routine to determine the optimum size of the memory." (e.g., see column 6, lines 43-47) for determining an optimized memory organization (how many memories, which size for each memory, interconnection patterns of said memories), such that the digital device can run with optimal performance (for instance with minimal power consumption). The motivation for combining the two references is based on the same rational given in rejection of claim 1.

: IMPORTANT NOTE :

*If the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to **amend the title of the invention** such that it is descriptive of the invention as claimed as required by sec. **606.01** of the **MPEP**. Furthermore, the **summary of invention** and the **abstract** should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of **sec. 1302.01** of the **MPEP**.*

*As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See **37 C.F.R. § 1.111(b)** and **§ 707.07(a)** of the **M.P.E.P.***

Response to Applicant's Remarks

The Examiner notes that the Applicant has included the allowable subject matter in the independent claims. However, as mentioned above in view of discovery of the new prior art reference the previously allowed claims have been rejected. The Examiner apologizes if this rejection will cause any inconvenience.

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent Publication No. 2003/0145239 to Kever et al. describes Dynamically adjustable cache size based on application behavior to save power.

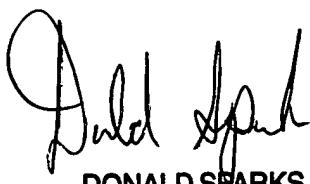
2. U. S. Patent No. 5,761,715 to Takahashi describes Information processing device and cache memory with adjustable number of ways to reduce power consumption based on cache miss ratio.
3. U. S. Patent Publication No. 2003/0061448 to Rawson, III describes Selectively powering portions of system memory in a network server to conserve energy.
4. U. S. Patent No. 2003/0236948 to Erdner et al. describes Cache way replacement technique.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from 8:00 AM to 5:00 PM.

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF
HF

2005-12-19



DONALD SPARKS
SUPERVISORY PATENT EXAMINER